

PATENTAttorney Docket No.: 10008023-1
U.S. Patent Application Serial No.: 09/982,020**REMARKS**

Favorable reconsideration of this application is respectfully requested in view of the amendments above and the following remarks. Claims 1 and 18 have been amended. Claims 2, 19, 28, and 30 were previously canceled without prejudice or disclaimer of the subject matter contained therein. Claims 1, 3-18, 20-27, 29 and 31 are pending, of which claims 1, 18 and 25 are independent.

Claim 18 has been rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by MacLeod (6,090,156).

Claims 1, 3-17, 20-27, 29, and 31 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over MacLeod in view of Sato (5,261,062).

These rejections are respectfully traversed for at least the reasons set forth below.

Office Interview Dated March 30, 2006

An office interview between the Examiner and Tiep Nguyen, Reg. No. 44,465 was conducted on March 30, 2006. In the interview, Mr. Nguyen explained the differences between the alleged prior art, MacLeod, and independent claims 18 and 25. Particularly, it was pointed out to the Examiner that MacLeod at FIG. 1 and associated text clearly show an optimizer 4 acting on the intermediate code subsequent to the generation of such intermediate code at the parser 2 and prior to the register allocation at the register allocator 6. In contrast, claim 18 recited allocating the real registers *while* generating the intermediate code (which has been clarified to recite "during the step of generating the intermediate code"), and claim 25 recites a register allocation stage that is configured to both generate the intermediate code and allocate the real registers.

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In the interview, the Examiner contended that the language of claim 18 broadly states, "allocating a plurality of real registers ... while generating the intermediate code;" thus, the claimed "generating the intermediate code" does not refer back to the previously claimed step of "generating intermediate code from a portion of source code." Next, the Examiner contended that the rewriting of the already-generated intermediate code to merely substitute the symbolic registers with the allocated real registers as shown in MacLeod at step 24 in FIG. 2 reads on the claimed "generating the intermediate code." The Examiner's contention is illogical and deviates from the clear language of claim 18. However, in the interest of expediting the prosecution of the application, claim 18 has been amended to clearly recite "allocating a plurality of real registers ... during the step of generating the intermediate code" in order to clearly refer back to the previous step of "generating intermediate code from a portion of source code."

Regarding claim 25, the Examiner provided no explanation in the interview as to how MacLeod could be read on the claimed register allocation stage that is configured to both generate the intermediate code and allocate the real registers, especially when MacLeod's FIG. 1 clearly shows separate elements for generating the intermediate code (parser 2) and allocating real registers (register allocator 6), with an optimization stage (optimizer 4) therebetween.

In the interview, the Examiner indicated that she will: a) consult with her supervisory examiner or an appropriate primary examiner to discuss the aforementioned differences between MacLeod and claims 1, 18, and 25 and amendments to claims 1 and 18 as proposed by Mr. Nguyen; and b) provide a response the following day, March 31, 2006. As of the

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filng date of this Amendment on April 3, 2006 to avoid late filing fees, the Examiner has not responded.

Claim Rejection under 35 U.S.C. § 102

The test for determining if a reference anticipates a claim, for purposes of a rejection under 35 U.S.C. § 102, is whether the reference discloses all the elements of the claimed combination, or the mechanical equivalents thereto functioning in substantially the same way to produce substantially the same results. As noted by the Court of Appeals for the Federal Circuit in *Lindemann Maschinenfabrik GmbH v. American Hoist and Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984), in evaluating the sufficiency of an anticipation rejection under 35 U.S.C. § 102, the Court stated:

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.

Therefore, if the cited reference does not disclose each and every element of the claimed invention, then the cited reference fails to anticipate the claimed invention and, thus, the claimed invention is distinguishable over the cited reference.

Claim 18 has been rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by MacLeod (6,090,156).

As mentioned earlier, claim 18 has been amended to clearly recite, *inter alia*, "allocating a plurality of real registers ... during the step of generating the intermediate code." In contrast, MacLeod at FIG. 1 and associated text clearly shows a parser 2 generating the intermediate code *prior* to the register allocator 6 allocating the real registers, with an optimizer 4 therebetween.

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Accordingly, it is respectfully submitted that claim 18 is not anticipated by MacLeod, and withdrawal of the rejection of this claim is respectfully requested.

Claim Rejections Under 35 U.S.C. §103(a)

The test for determining if a claim is rendered obvious by one or more references for purposes of a rejection under 35 U.S.C. § 103 is set forth in MPEP § 706.02(j):

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Therefore, if the above-identified criteria are not met, then the cited reference(s) fails to render obvious the claimed invention and, thus, the claimed invention is distinguishable over the cited reference(s).

Claims 1, 3-17, 20-27, 29, and 31 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over MacLeod in view of Sato (5,261,062).

Claims 1 and 3-17

Claim 1 has been amended to recite, *inter alia*, "optimizing the intermediate code subsequent to the step of selecting the class of real registers." In contrast, MacLeod at FIG. 1 and associated text show an optimizer for optimizing the intermediate code *prior* to the

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register allocator 6 allocating or selecting the class of real registers. Furthermore, the Office Action did not rely Sato to make up for the aforementioned deficiencies in MacLeod.

Accordingly, it is respectfully submitted that the Office Action failed to establish a *prima facie* case of obviousness against claim 1 and its dependent claims 3-17 as they now stand. Withdrawal of the rejection of these claims and their allowance are, therefore, respectfully requested.

Claims 18 and 20-24

It is respectfully submitted that, for at least the reasons set forth earlier, claims 18 and 20-24 are not anticipated by MacLeod. In addition, the Office Action does not rely upon Sato to make up for the deficiencies in MacLeod with respect to claims 18 and 20-24.

Accordingly, it is respectfully submitted that the Office Action failed to establish a *prima facie* case of obviousness against claim 18 and its dependent claims 20-24 as they now stand. Withdrawal of the rejection of these claims and their allowance are, therefore, respectfully requested.

Claims 25-27 and 29-31

Regarding claim 25, as discussed earlier, it recites, "a register allocation stage configured to generate intermediate code ... and configured to allocate a plurality of real registers" and an "optimization stage configured to optimize said intermediate code." In contrast, MacLeod clearly shows a parser 2 stage for generating intermediate code and a register allocator 6 stage for allocating real registers, whereby the two stages are separate

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from each other by an optimizer stage 4. Furthermore, the Office Action did not rely on Sato to make up for the aforementioned deficiencies in MacLeod.

Accordingly, it is respectfully submitted that the Office Action failed to establish a *prima facie* case of obviousness against claim 25 and its dependent claims 26, 27, 29, and 31 they were previously presented. Withdrawal of the rejection of these claims and their allowance are, therefore, respectfully requested.

Conclusion

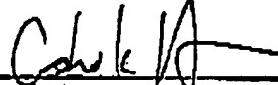
In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

Dated: April 3, 2006

By



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